

Wafer-to-Wafer Bonding for Microstructure Formation

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Invited Paper

Wafer-to-wafer bonding processes for microstructure fabrication are categorized and described. These processes have an impact in packaging and structure design. Processes are categorized into direct bonds, anodic bonds, and bonds with intermediate layers. Representative devices using wafer-to-wafer bonding are presented. Processes and methods for characterization of a range of bonding methods are discussed. Opportunities for continued development are outlined.

Keywords—Anodic bonding, MEMS, micromachining, silicon direct bonding, silicon fusion bonding, wafer bonding.

I. INTRODUCTION

Micromachining encompasses a broad range of technologies anchored in the core technology of microlithographic pattern transfer. A large fraction of the micromachining technologies are specific to the silicon material system principally due to the origins of the field, namely, the silicon integrated circuit (IC) industry. In the silicon micromachining field, there have been two dominant fabrication methods, broadly classified as bulk micromachining (etching deep features into a wafer) and surface micromachining (depositing, patterning, and selective etching of films on a wafer). Fundamentally, both of these techniques rely on some form of etching or material removal. A complementary, additive, micromachining technology is the wafer-to-wafer bonding of patterned substrates, often simultaneously involving alignment of the substrates.

Historically, some of the earliest uses of wafer-to-wafer bonding were for packaging of pressure sensors. These wafer-to-wafer bonds were performed at low temperatures (less than 450°C) and involved either field-assisted silicon-to-glass bonding (anodic bonding) or a eutectic bond between silicon wafers using a gold thin film. The advantage of the low temperatures of these bonds was that wafers with common IC metals such as Al could withstand this temperature without degradation. More recently, techniques

for the direct bonding of smooth, flat wafers without field assist or intermediate layers have emerged. These bonding methods offer the advantage in some circumstances of being high-temperature stable bonds, thus permitting a wide range of subsequent processes. Additionally, the silicon-silicon direct bonds produce structures with far less thermal expansion mismatch problems when compared to anodic or eutectic bonding. The emergence of these techniques has catalyzed a great deal of activity in wafer-to-wafer bonding for a range of applications. We will review examples of uses of wafer-to-wafer bonding in microstructure formation in the next section, and then review the specific bonding methods.

It is worth noting that a comprehensive review of bonding techniques for microsensors was written by W. H. Ko *et al.* in 1985 (predating the silicon direct bonding activity) [1]. Additionally, other reviews of silicon direct bonding have been given for both microelectronic and microstructure applications [2]–[4]. Last, there has been a series of four proceedings volumes for the International Symposium on Wafer Bonding held since 1991 as part of the Electrochemical Society Meetings [5]–[8]. This paper will attempt to compliment these existing reference bodies, with an emphasis on the more recent activities and their relevance to microsystems.

II. THE ROLE OF BONDING IN MICROSTRUCTURE FORMATION

As was mentioned in the previous section, one of the earliest uses of wafer-to-wafer bonding was in the packaging of pressure sensors. An example of this is shown in the schematic cross section of Fig. 1, which is an illustration of a Motorola pressure sensor [9]. In this example, a wafer-level bond is performed to produce a reference vacuum cavity for an absolute pressure sensor. The wafer-to-wafer bond illustrated in this figure is a thin-film glass frit bond. The pressure sensor has been fabricated using bulk micromachining and thin-film processes for the piezoresistors. In the case of a gauge pressure sensor, the

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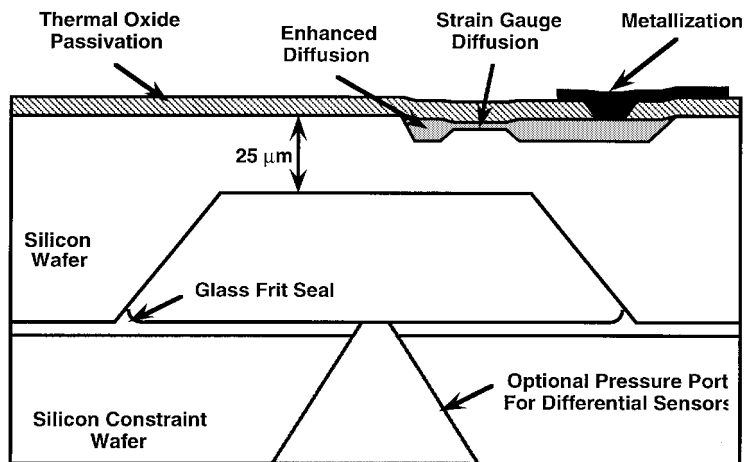


Fig. 1. A Motorola pressure sensor using glass frit wafer bonding for packaging [9].

lower wafer is etched to form an inlet port, and thus the role of the lower wafer bond reverts from that of a vacuum seal to a first-level pressure inlet manifold. In either case, the primary function of the wafer bonding is to effect a package function.

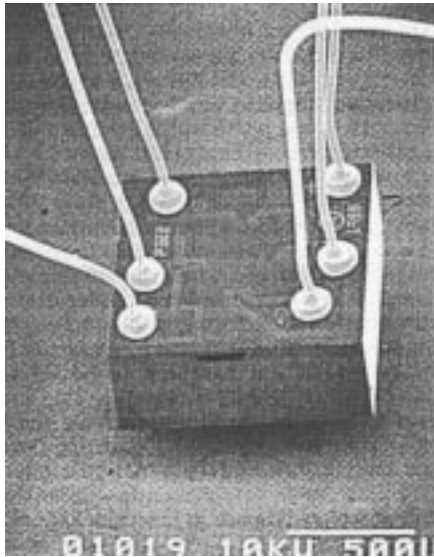
This raises an important point, namely, the concept of *wafer-level packaging*. It is readily acknowledged, particularly in the sensors industry, that packaging can be a dominant component in the final manufactured cost of a device. By achieving package function at the wafer level, it is possible to realize tremendous overall savings in cost since this enables the packaging of a multitude of sensors or actuators simultaneously, eliminating costly individual chip-packaging steps.

Another example of the use of wafer bonding in the manufacture of pressure sensors is shown in Fig. 2 [10]. Here, the pressure sensor is formed by a high-temperature silicon direct bond, followed by thinning of a wafer and fabrication of the piezoresistors. In comparison with the conventional bulk micromachined pressure sensor of Fig. 1, this pressure sensor has several interesting features that are enabled by the wafer bonding. The wafer bonding produces a reference cavity for the absolute pressure sensor as in the previous case; however, the cavity depth can be made considerably smaller ($1\text{--}10\ \mu\text{m}$) as compared to the bulk micromachined devices ($\sim 500\ \mu\text{m}$). The benefit of this is that the lower surface of the sealed cavity can function as an overpressure stop. In the event of a large pressure, the sensing membrane can be designed to “bottom out” against the cavity lower surface, preventing catastrophic failure of the pressure sensor. Again, we see the bonding’s providing a package function at the wafer level, as well as being responsible for the definition of the core element of the device (the sensing membrane). There are several other noteworthy advantages of this device. Typically, a bulk micromachined pressure sensor is limited to chip sizes greater than 1 mm because of the sloped sidewalls of the anisotropically etched silicon wafer. In the case of this device, it is possible to realize a much smaller chip ($\sim 200\ \mu\text{m}$). Also, the membrane edge length is defined by a

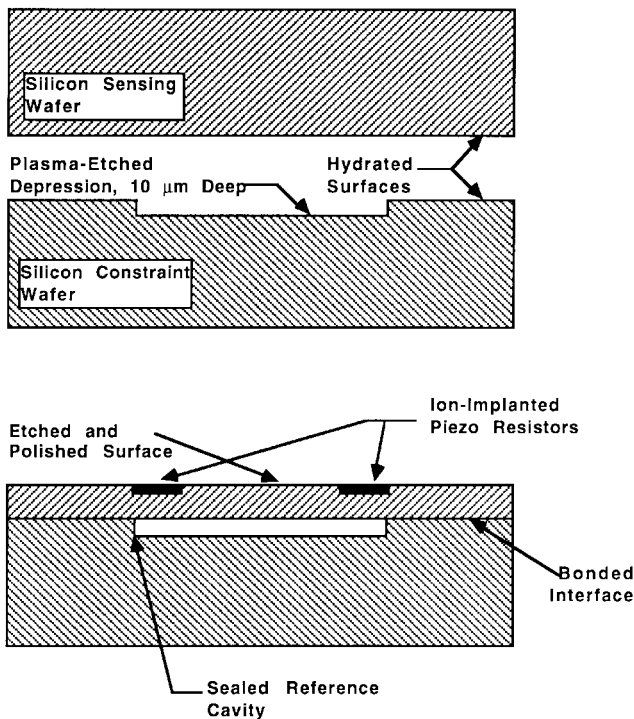
shallow plasma etch, which has much better dimensional control than the bulk micromachined device where the wafer thickness has a direct impact on the membrane edge length. Last, the membrane can be made circular, which is often desirable from a strength standpoint but not attainable in the case of the bulk micromachined device. It is also possible to realize a similar type structure utilizing polysilicon surface micromachining [11], but the wafer-bonding approach provides a single crystal silicon membrane, which generally gives better mechanical property control and permits diffusion of piezoresistors.

A multitude of other interesting examples of sensors built using wafer bonding exist. One noteworthy early example is that of an accelerometer in which the bonding not only defines the critical mechanical flexures in the device but also is used to implement overacceleration stops for the proof mass. This greatly enhances the manufacturability and packaging of the device, shown in Fig. 3 [12].

Another important role for wafer bonding is in the creation of multiwafer laminations, often to form fluidic elements. The simplest form of a wafer-bonded fluidic device is a flow channel, formed by etching one or both substrates with flow channels and through-holes, followed by the wafer-to-wafer bond, illustrated in the case of a silicon-to-glass bond in Fig. 4. This type of bonded structure has been realized in many forms for a wide range of applications, from inkjet print heads to biomedical devices and micro total analytical systems [13]–[15]. In most instances, very sophisticated fluidic devices can be realized, such as mixers, with just two wafers [16]. Nonetheless, more complicated devices have been realized using wafer bonding of a multitude of substrates. These include four wafers bonded together to form an electrostatic valve [17], or more than 20 wafers bonded together to create a complicated microchemical reactor [18], as shown in Fig. 5. Ultimately, the ability to perform aligned laminations of a large number of patterned wafers is likely to have a large impact on fluidic devices. Concepts for high-speed rotating machinery based on seven wafer-bonding operations are also being explored [19].



(a)



(b)

Fig. 2. A silicon wafer-bonded pressure sensor. (a) Die photo. (Courtesy of Lucas NovaSensor [10].) (b) Cross section of process.

III. CATEGORIES OF WAFER-TO-WAFER BONDING

The types of wafer bonding that are most commonly employed in microstructure fabrication can be placed in three categories:

A. Direct Bonds

Wafers are directly contacted without the assistance of significant pressure or any intermediate layers or fields. These bonding schemes rely on the tendency for smooth surfaces to adhere, and always utilize some form of thermal cycling after the contacting to increase the bond strength.

The maximum temperature of the anneal defines the bonding as being low temperature ($<450^{\circ}\text{C}$) or high temperature ($>800^{\circ}\text{C}$).

B. Anodic Bonds

The wafers are contacted and the bond is completed by application of an electric field at temperatures in the range of $300\text{--}450^{\circ}\text{C}$. The bond is typically performed between a sodium-baring glass wafer and a silicon wafer.

C. Intermediate-Layer Bonds

This category includes all bonding mechanisms that require an intermediate layer to promote the wafer bond. This could include eutectic bonds, polymers, solders, or thermo-compression bonds. Many of these wafer-level bonds are a scale-up of bonds that have been routinely performed at the die level in the packaging of IC's.

The next sections will discuss each of these bonding methods in detail. The emphasis will be placed on silicon direct bonding.

IV. DIRECT BONDING

A. Background

The direct-bond method relies on forces that naturally attract surfaces together when they are very smooth and flat. A range of mechanisms have been proposed to explain this initial contact attractive force. It is well known that smooth metal surfaces, if atomically clean, will bond together. This process is often referred to as “cold welding” and is typically achieved by cleaning and contacting the metal surfaces in vacuum to maintain cleanliness. This bond usually relies on plastic deformation of the metal to bring the atoms in close contact. In the case of most direct bonds that have been performed for microstructures, some surface treatment (e.g., hydration, oxygen plasma exposure) is conducted prior to the contacting to promote the surface attraction and bonding process. This is sometimes assisted by a modest pressure to expel air from between the wafers and to initiate the contact. The bond is usually followed by a thermal cycle, which increases the strength of the bond. In the following sections, we will begin with a description of the silicon direct bonding process, discuss characterization methods for the silicon bond that generalize to all bonding methods, and investigate bonding methods for other types of substrates.

B. Silicon Bonding Process

Extensive review articles have been written on the silicon wafer-bonding process, particularly as it pertains to electronic device fabrication [2], [4], [20]–[22]. This process has also been referred to as silicon fusion bonding. This section will simply summarize the major points of the process for the bonding of silicon or silicon dioxide surfaces. The silicon wafer-bonding process consists of three basic steps: surface preparation, contacting, and annealing. The starting wafers must be smooth and flat. There have been studies

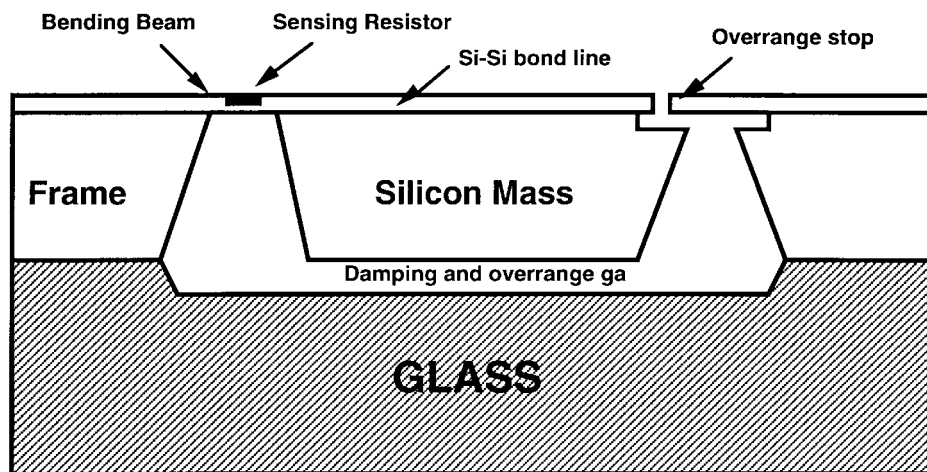


Fig. 3. A microaccelerometer using wafer bonding [12]. (Courtesy of Lucas NovaSensor.)

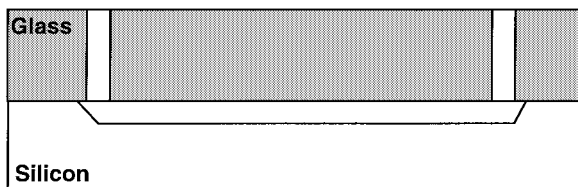


Fig. 4. Flow channels formed by silicon-glass bonding.

of the necessary surface quality for wafer bonding [23], [24], and in general, it has been experimentally observed that the wafers should have a roughness of no greater than about 10 \AA and a bow of less than $5 \mu\text{m}$ (on a $4''$ wafer). Also, protrusions from the surface (resulting from previous processing) of greater than 10 \AA can produce problems in the bonding. All of the process steps are conducted in a cleanroom environment, although Gösele has proposed a powerful "microcleanroom" concept that does not require a cleanroom [25]. The surface-preparation step involves cleaning the mirror-smooth, flat surfaces of two wafers to form a hydrated surface. There have been studies of the differences between hydrophobic and hydrophilic surfaces on the final bond interface [22]. Following this preparation, the wafers are contacted in a clean environment by gently pressing the two surfaces together at one central point. The surfaces come into contact at this point and are bound by a surface attraction of the two hydrated surfaces. A contact wave is initiated at this point and sweeps across the wafer surfaces, bringing them into intimate contact over the entire surface. The contacting process is critical to prevent trapping of particulate or air between the surfaces. The exact origin of the attractive force that promotes the contact wave is not universally agreed upon [22] and depends to a certain extent on whether the bond is Si-Si or Si-SiO₂. The most common assumption is that a bond is formed between -OH groups on the opposing surfaces.

The final step in the bonding process is an elevated temperature anneal of the contacted pair at temperatures anywhere from room temperature to 1200°C . While the room-temperature contacted samples are well adhered, this anneal

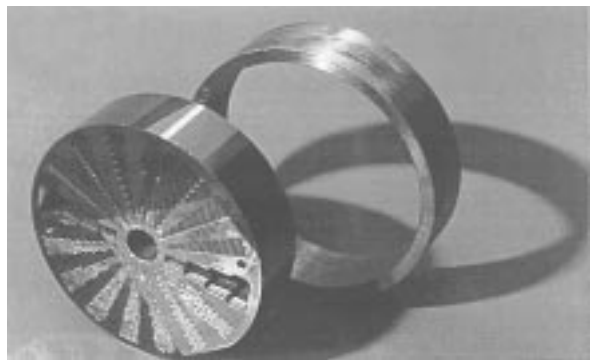


Fig. 5. A stack of 25 individually patterned wafers that have been aligned and bonded to form a micromachined chemical reactor [18]. (Courtesy of Dr. J. Ryley, DuPont.)

generally increases the bond strength by more than an order of magnitude at the higher temperatures ($800\text{--}1200^\circ\text{C}$). Measurements of the bond strength as a function of anneal temperature indicate three distinct regions. The first region, for anneal temperatures less than 300°C , exhibits a relatively constant bond strength equal to the bond strength of the wafers prior to anneal. At temperatures greater than 300°C , the bond strength increases and then levels out. It is presumed that an Si-O-Si bridging bond is formed between the surfaces and a water molecule is liberated. At temperatures greater than 800°C , the bond strength begins to increase again. In this third region, it has been suggested that surfaces can more easily deform (oxide flow) and trapped water may oxidize surfaces, bringing them into better contact. At temperatures of 1000°C or greater, the bond strength is in the range of the strength of the silicon crystal itself. Kinetically, the bond strength at high temperatures ($>800^\circ\text{C}$) seems to saturate within a few minutes at the anneal temperature. In lower temperature anneals, the bond strength has been observed to increase over very long times (days) [26], [67].

C. Bond Voids

When contacting and annealing a wafer pair, voids are sometimes observed upon inspection. These voids are gen-

erally lumped into two categories: extrinsic and intrinsic. The extrinsic voids are those created by particles, protrusions on the wafer surface, or trapped air. These voids are usually observed on contact and do not change significantly during annealing. Fig. 6 shows infrared (IR) transmission images of wafers with various forms of extrinsic voids (the imaging methods are described in the next section). Intrinsic voids are voids that are generated during the anneal cycle [4]. After contact, the wafer pair will appear void free. However, as the anneal temperature is increased, voids begin to appear above 400°C and subsequently disappear above 900°C. The voids usually are only seen when bonding silicon to silicon without an intermediate oxide, and they are often attributed to hydrocarbon contamination, although there is not a consensus on their origin. Gösele has provided some detailed discussion of this issue [67]. It has been observed that cavities in the wafers can serve to “getter” these microvoids, thus minimizing the problem [27], [28].

D. Bond Characterization

Several nondestructive and destructive techniques exist for mechanical characterization of the bonding process. In this section, we will discuss the methods as applied to silicon direct bonding, but many of these same techniques can be applied to other methods of bonding. The most common techniques are bond imaging, cross-sectional analysis, and bond-strength measurement. The imaging methods are nondestructive and can be used as in-process monitors, while the cross-sectional analysis and bond-strength measurements are destructive and require control wafers for characterization.

The three dominant methods for imaging a bonded pair of silicon wafers are infrared transmission, ultrasonic, and X-ray topography. Examples of the images obtained by these methods for two bonded 4-in silicon wafer pairs are shown in Fig. 6. A simplified schematic of an infrared imaging system is shown in Fig. 7. It consists of an IR source (typically an incandescent light bulb) and an IR-sensitive camera. A silicon charge-coupled device camera has sufficient sensitivity in the near-IR range that it can be used when outfitted with a filter for visible light. The bonded wafer pair is located between the source and camera. Any imperfection in the bond shows up as changes in contrast in the IR image. Large unbonded regions (“voids”) appear with a characteristic “Newton’s Rings” pattern. This imaging method generally cannot image voids with a separation of surfaces less than one-quarter of the wavelength of the IR source. Based on a typical particle void, this translates to a spatial resolution of several millimeters [24]. Fig. 8, which compares the three imaging methods using the same wafer, clearly illustrates voids not present in the IR image, which do show up in the other methods. Also, this technique works for silicon wafers of moderate doping level with smooth surfaces. Highly doped layers, IR absorbing films, or rough surfaces (backside of wafer) can limit the image quality. In spite of this resolution limit, the IR method has the advantage

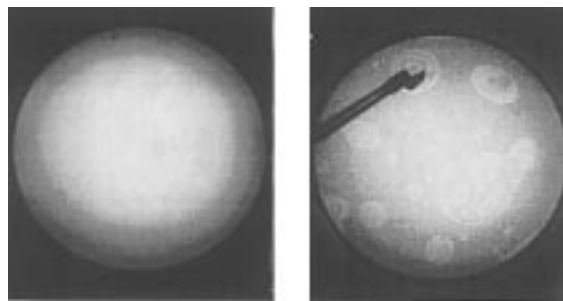


Fig. 6. IR transmission image of two bonded wafer pairs. The pair on the right has several voids at the bonded interface due to particles and trapped air.

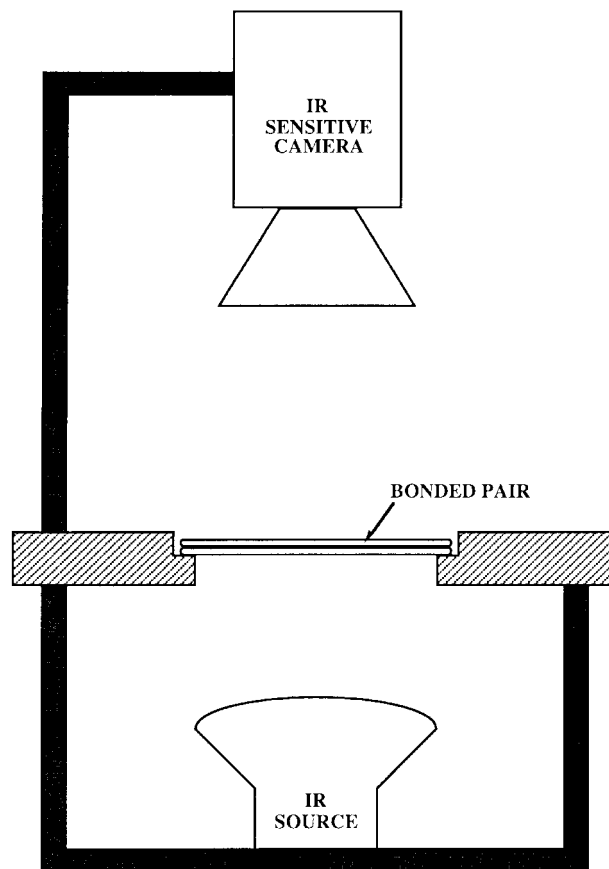


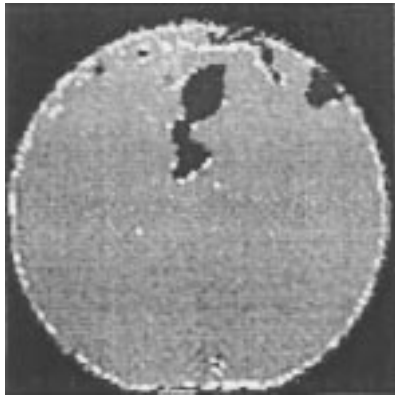
Fig. 7. Schematic illustration of the IR imaging system.

of being simple, fast, and inexpensive. It can be used directly in the cleanroom to image the wafers before and after anneal. The other two imaging methods offer higher resolution at the expense of speed, cost, and incompatibility with cleanroom processing.

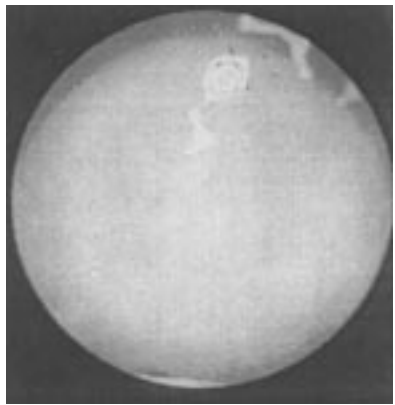
Cross-sectional analysis can be performed at the bonded interface by cleaving the sample. Scanning electron microscope (SEM) and transmission electron microscope techniques have been used to image the bonded interface at a submicrometer scale. These studies have helped to understand the composition of the bonded interface [22]. Additionally, it is possible to gain a great deal of information about the bonded interface by simply defect etching the cross-sectioned sample. Several groups have demonstrated



(a)



(b)



(c)

Fig. 8. Comparison of three methods for visualization of the same bonded wafer pair. (a) X-ray topograph. (b) Ultrasonic. (c) IR transmission. (X-ray and ultrasound courtesy of Dr. T. Abe, SEH-Japan.)

the benefit of this approach, particularly for visualization of voids on the order of tens of micrometers (“microvoids”) [29].

The bond strength has been characterized by a number of techniques. Fig. 9 highlights the most common techniques. Pressure burst tests [Fig. 9(a)] can often yield a number that has engineering significance in the design of sensors but yields little information about the detailed nature of the bond due to the complicated loading of the interface. A tensile/shear test sample [Fig. 9(b)] gives better information on the bonded interface but is often limited by difficulties

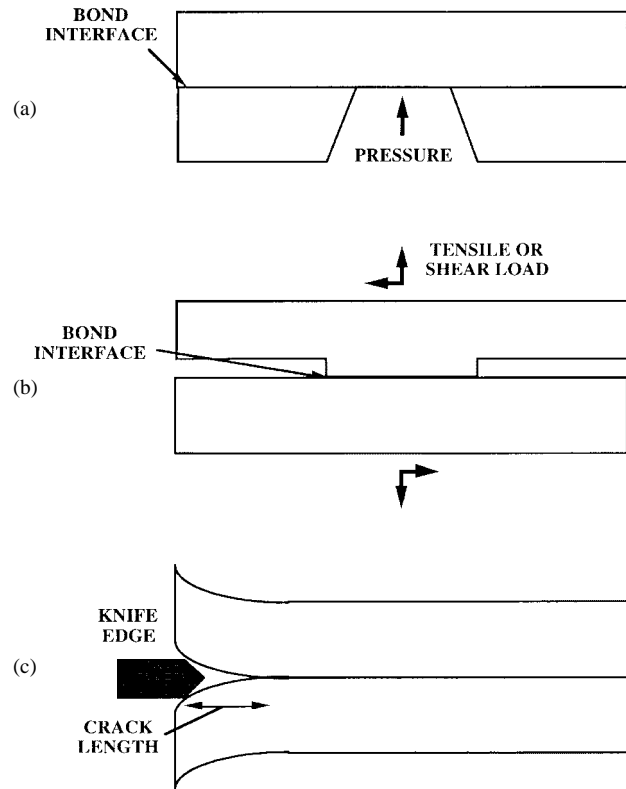


Fig. 9. Bond strength measurement techniques.

in loading and sample handling [30]. The knife-edge, or double cantilever, technique [Fig. 9(c)] has the advantage of creating a very well-defined loading on the bonded interface. A blade of defined thickness is inserted between the bonded pair in a region where a crack has been initiated. Using IR imaging methods, the length of the crack is measured, from which the surface energy can be inferred through a knowledge of the sample and blade thicknesses and the elastic properties of the wafer [31]. This method has been used with very good success. It has been noted, however, that the crack length is time (and humidity) dependent, and thus caution must be exercised in conducting this measurement [67]. Unfortunately, the surface energy is fourth power dependent on the crack length, and thus uncertainties in the crack length produce large uncertainties in the extracted surface energy. Other methods based on patterned samples have been proposed to eliminate this problem for silicon direct bonding [32] and silicon-glass anodic bonding [33].

E. Sealed Cavity Effects at High Temperature

Nearly all micromechanical applications of silicon wafer bonding require bonding of wafers with cavities etched in one or the other wafer, thus forming sealed cavities in the wafer after the bond. The nature of gases that exist in the cavities can be very important, particularly in subsequent high-temperature bonding. It has been shown that when wafers are contacted in air, and subsequently annealed at high temperature, the oxygen in the cavity can react with the silicon surface and create a partial vacuum [34].

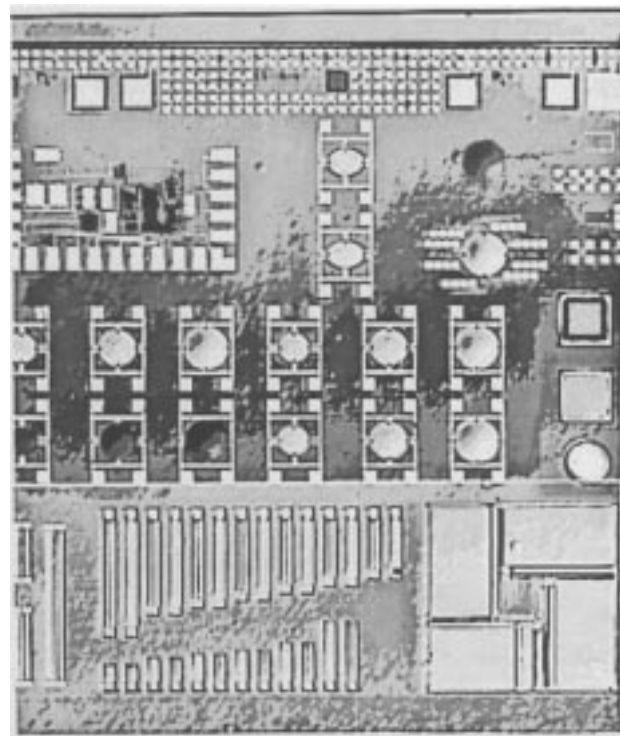
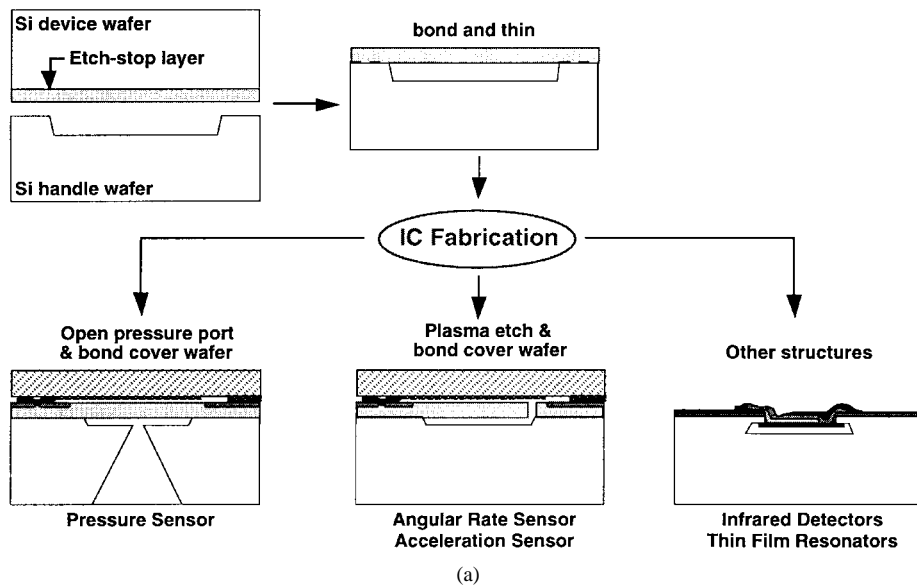


Fig. 10. (a) A method for integration of electronics and mechanical devices using wafer bonding. (b) SEM micrograph of a test chip containing accelerometers, pressure sensors, and complementary metal-oxide-semiconductor integrated circuits by this process. (Courtesy of C. Hsu and L. Parameswaran.)

When the oxygen is completely consumed (for shallow cavities), the resultant pressure inside the cavity is 0.8 atm, consistent with the consumption of the 20% oxygen in air. These results indicate that the bonding process forms rapidly enough that it can trap gasses in the cavities. Under high temperatures, the residual gases trapped in the cavities can induce plastic deformation in thin silicon membranes as the gases expand [34]. This problem can be reduced or eliminated by controlling the ambient under

which the wafers are contacted. We have demonstrated that the pressure inside the cavity can be reduced by bonding the wafers in an oxygen-rich ambient [35]. Alternatively, it is possible to bond the wafers in a vacuum.

By controlling the bonding ambient, a wide range of microstructures can be realized that permit high-temperature operations following the bond. One example is the formation of integrated sensors by processes such as those illustrated in Fig. 10. This general process has been suc-

cessfully demonstrated by a number of groups [36]–[38]. Recently, the merger of deep reactive ion etching and sealed cavity wafer bonding has opened an exciting area of microelectromechanical systems devices [39].

F. Bonding of Nonsilicon Materials

While the previous sections have discussed bonding of silicon wafers, the same basic process steps can be applied to bonding a variety of materials [67]. Quartz wafers can be bonded by this method [14]. Examples of bonding of dissimilar materials include the bonding of GaAs to Si [40] and Si to glass [41]. Provided the surfaces are mirror smooth and can be hydrated, the bonding proceeds in a fashion identical to Si–Si bonding. Bonding of III–V compounds has been achieved at temperatures of 500°C in a hydrogen atmosphere [67]. When bonding dissimilar materials, the major complication is stresses generated during the high-temperature anneal due to differences in thermal coefficient of expansion of the two materials [41].

Bonding has also been demonstrated for samples with deposited films. Examples of bonding to silicon wafers with deposited polysilicon or silicon nitride have been reported [42]–[44]. Polishing is often needed to establish the necessary level of roughness.

G. Low-Temperature Direct Bonds

Most demonstrations of direct bonding have required high-temperature anneals, which precludes their use with metalized wafers. Because of the potentially significant benefit in packaging of sensors, increased interest has focused on lower temperature direct bonding methods. A variety of approaches have been proposed [26], [28], [45]–[50], [67], most of which involve some modification of the surface preparation to enhance the initial surface attraction.

V. ANODIC BONDING

The field assisted bond was initially developed for the bonding of metal to glass, and subsequently the metal was replaced by silicon [1], [51]–[58]. The anodic bonding process is shown schematically in Fig. 11 in the case of silicon-to-glass bonding. The glass wafer is biased as the cathode, and the silicon wafer is the anode. The contacted wafers are heated to 300–400°C while a voltage of approximately 200–1000 V is applied. Under such a high field and elevated temperature, the mobile Na ions in the glass migrate away from the bonded interface, leaving behind fixed charge in the glass that creates a high electric field across the bond interface with image charges in the silicon. At these temperatures and electric fields, a chemical bond is presumed to occur that fuses the wafers together. Many of the same conditions for contacting from silicon direct bonding apply to this process, although the process is more tolerant of surface roughness due to the high forces of attraction created by the electric field. The primary variables that control this process are temperature, time, and voltage. A great deal of attention is paid to ensure that the glass has a

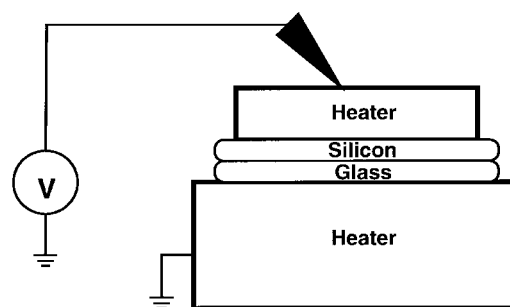


Fig. 11. Anodic bonding apparatus.

good thermal coefficient of expansion fit to silicon. Several glass fabricators now market glasses that are specifically designed to have a good match to silicon for this process. One method to minimize the thermal stress effects is to utilize a sputtered glass layer on a silicon wafer, such that the substrates being bonded are both silicon, and thus the thermal mismatch would only be caused by the thin glass [1], [59]. The silicon wafer with sputtered glass is thus contacted to a bare silicon wafer, and the temperature and voltages are applied. One additional benefit of the sputtered glass layer approach is that the applied voltage may be reduced, which is sometimes critical to prevent damage to electronic components that might be on the wafers.

In addition to the examples cited in the earlier section for applications of this bonding approach, the anodic bond has been critical to the dissolved wafer process pioneered at the University of Michigan [60]. The dissolved wafer process has been used successfully for a wide range of devices, such as pressure sensors, flow sensors, and inertial devices.

VI. INTERMEDIATE-LAYER BONDING

A wide range of intermediate layers have been used for wafer-to-wafer bonding in microstructure fabrication. These approaches include:

- eutectic (using Au thin films) [1], [61];
- solder (using thin-film deposited solders or preforms) [1], [62];
- polymer [63];
- low melting temperature glasses (including glass frits) [1], [4];
- thermocompression (using soft metal thin films) [35], [64], [65].

The eutectic bond was explored extensively by Ko and coworkers for the packaging of pressure sensors. Some drift mechanisms were identified in pressure sensors that were attributed to this bond [1]. Solder bonding has been employed successfully for several different applications, including recently a novel scheme for microshell encapsulation [62]. Polymer bonds have been used extensively as temporary bonding agents, as in [63]. Glasses with a low melting temperature are a demonstrated production-worthy bond for pressure sensors in which the glass frit is typically screen printed [1].

The thermocompression bond is a relatively little-used wafer-level bonding mechanism that is intriguing for low-temperature vacuum bonding applications since it in principle would have very little outgassing, as compared to glasses, solders, or polymers. The process is analogous to the cold welding process, but temperature, pressure, and low hardness metals are used to combat surface contamination and surface oxides. The bonding process starts with the deposition of approximately 1- μm -thick Au layers with a suitable adhesion layer (Cr, Pt, Pd) on each wafer to be bonded. The wafers are cleaned using an ultraviolet-ozone clean to remove organic surface contaminants. After this, the wafers are aligned and contacted. In the process we run at the Massachusetts Institute of Technology (MIT), we apply 20 psi of pressure on the bonded area for 2.5 min at approximately 300–350°C [35], [64]. The bond has been tested in lap shear and has bond strengths comparable to that of wire bonds. Recently, a metal structure transfer process has been demonstrated that utilizes a similar process [65].

VII. CHALLENGES AND FUTURE DIRECTIONS

A great deal of progress has been made in recent times to advance wafer-to-wafer bonding as a viable production process for the manufacture of microstructures. As was described in the beginning of this paper, the primary driver for consideration of wafer-to-wafer bonding is the ability to incorporate a *wafer-level package function*. The potential benefit of this is most significantly felt in either higher performance or reduced cost. Another benefit of wafer-to-wafer bonding is in the realization of a mechanical structure that is otherwise unattainable, such as some of the highly three-dimensional structures that can be realized by multiwafer stacks. To realize the potential of wafer-to-wafer bonded structures fully, continued progress is needed in several areas.

First, a healthy infrastructure of equipment vendors that can supply wafer-to-wafer bonding process solutions to manufacturers must be nurtured. Currently, there are two companies that offer high-quality wafer-bonding process tools (Karl Suss and Electronic Visions). Typically, these tools permit alignment of wafers to within a few micrometers and contacting and annealing under a host of conditions: pressure, temperature, and controlled ambient (Fig. 12). Standardization of processes for these tools, and characterization of interactions between the process and the tools, are needed to develop confidence in investments in the manufacturing of devices. Industry-standard benchmarking for yield and cleanliness is needed for the typical processes.

A second area of focus is in the development of robust criteria for “bondability.” There exists a certain amount of conflicting information in the literature today on the criteria needed to achieve acceptable bonding. Some of this confusion results from different measurement standards for bonding (and different requirements). A standardized set of metrology methods would go a long way toward permitting rational comparison of processes for wafer-to-

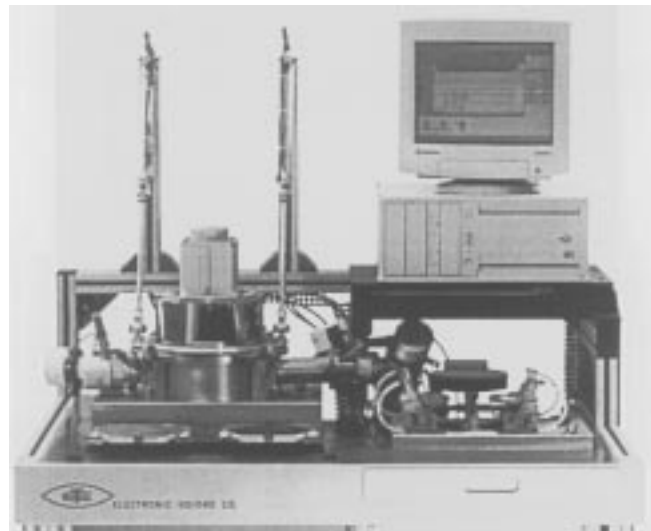


Fig. 12. A commercial wafer-bonding tool, which includes a chamber for controlled ambient bonding with temperature and pressure. (Courtesy of Electronic Visions Co.)

wafer bonding. As an example, a wide range of destructive methods are employed to measure bond strength. Unfortunately, many of these methods are strongly influenced by handling and mounting procedures, thus preventing statistically significant comparisons.

A third area of work is the characterization of stresses in bonded structures, and the long-term reliability of stresses that might result from a wafer-to-wafer bond. These effects are of primary importance in high-performance applications, and limited work has been done to date to understand the interaction of processes and materials in this area.

A fourth area is the development of techniques for bonding of dissimilar materials. This process capability opens up a wide range of potential new devices and structures. Management of thermal stresses and optimization of the bond strength are perhaps the greatest challenges in this area.

Last, there is a great opportunity for wafer-to-wafer bonding to achieve vacuum levels that are adequate for resonant or inertial sensors. Given the potential market for inertial devices, a robust means to package these in vacuum when needed could have a very large impact on the cost and performance of these devices. Some work has been done in this area already, but challenges exist to drive the vacuum levels to 1 mTorr and below for long lifetimes (ten years). Esashi and coworkers have recently shown some interesting results by utilizing nonevaporable getters [66]. This approach opens new challenges in bonding processes, getter fabrication and materials, and the equipment needed to accomplish the bond.

VIII. CONCLUSION

The wafer-to-wafer bonding processes that have been developed for microstructure fabrication have a very significant impact on manufacturing of devices for sensing and actuation. Some wafer-to-wafer bonding processes are already well-established production processes, and others

are poised to advance the capability to realize new classes of devices. The most significant area of application for this technology is in wafer-level packaging. A wide range of materials and technologies exist. Challenges remain to convert some of the new, promising technologies into accepted production techniques.

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